

**Inventor Name Search Result**

Your Search was:

Last Name = MOON

First Name = YONGSAM

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">08920336</a>	<a href="#">5955929</a>	150	08/27/1997	VOLTAGE-CONTROLLED OSCILLATOR RESISTANT TO SUPPLY VOLTAGE NOISE	MOON, YONGSAM
<a href="#">09007707</a>	<a href="#">5969552</a>	150	01/15/1998	DUAL LOOP DELAY-LOCKED LOOP	MOON, YONGSAM
<a href="#">09234777</a>	<a href="#">6600771</a>	150	01/20/1999	SPREAD SPECTRUM PHASE MODULATION FOR SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS	MOON, YONGSAM
<a href="#">09948123</a>	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	MOON, YONGSAM
<a href="#">10305254</a>	Not Issued	161	11/25/2002	0.6-2.5 GBaud CMOS tracked 3X oversampling transceiver with dead zone phase detection for robust clock/data recovery	MOON, YONGSAM
<a href="#">10356695</a>	<a href="#">6859107</a>	150	01/30/2003	FREQUENCY COMPARATOR WITH HYSTERESIS BETWEEN LOCKED AND UNLOCKED CONDITIONS	MOON, YONGSAM
<a href="#">10612840</a>	Not Issued	30	07/03/2003	Tracked 3X oversampling receiver	MOON, YONGSAM
<a href="#">10613442</a>	<a href="#">6888417</a>	150	07/03/2003	VOLTAGE CONTROLLED OSCILLATOR	MOON, YONGSAM
<a href="#">10651500</a>	Not Issued	41	08/29/2003	CMOS transceiver with dual current path VCO	MOON, YONGSAM
<a href="#">10652721</a>	Not Issued	160	08/29/2003	CMOS transceiver with dual current path VCO	MOON, YONGSAM
<a href="#">10722842</a>	<a href="#">6876240</a>	150	11/25/2003	WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP	MOON, YONGSAM
<a href="#">60026106</a>	Not Issued	159	08/27/1996	SUPPLY NOISE INDEPENDENT VOLTAGE CONTROLLED OSCILLATOR	MOON, YONGSAM
<a href="#">60071805</a>	Not Issued	159	01/20/1998	SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS THROUGH SPREAD SPECTRUM PHASE MODULATION	MOON, YONGSAM
<a href="#">60230589</a>	Not Issued	159	09/05/2000	Oversampling transceiver with dead-zone phase detection	MOON, YONGSAM
<a href="#">60333439</a>	Not Issued	159	11/26/2001	0.6-2.5GBaud CMOS tracked 3x oversampling transceiver with dead-zone phase detection for robust clock/data recovery	MOON, YONGSAM
<a href="#">60406858</a>	Not Issued	159	08/29/2002	CMOS transceiver with dual current path VCO	MOON, YONGSAM
<a href="#">60590710</a>	Not Issued	159	07/22/2004	Divide-by-16.5 frequency divider with cascaded divide-by-3 and divide-by-5.5 dividers and devices including same	MOON, YONGSAM

Inventor Search Completed: No Records to Display.

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**Inventor Name Search Result**

Your Search was:

Last Name = AHN

First Name = GIJUNG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">09146818</a>	<a href="#">6229859</a>	150	09/04/1998	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	AHN, GIJUNG
<a href="#">09234619</a>	<a href="#">6560290</a>	150	01/20/1999	CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABAUD SPEED DATA COMMUNICATION	AHN, GIJUNG
<a href="#">09814256</a>	<a href="#">6587525</a>	150	03/21/2001	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	AHN, GIJUNG
<a href="#">09948123</a>	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	AHN, GIJUNG
<a href="#">10171860</a>	<a href="#">7088398</a>	150	06/14/2002	METHOD AND APPARATUS FOR REGENERATING A CLOCK FOR AUXILIARY DATA TRANSMITTED OVER A SERIAL LINK WITH VIDEO DATA	AHN, GIJUNG
<a href="#">10192296</a>	<a href="#">6914637</a>	150	07/10/2002	METHOD AND SYSTEM FOR VIDEO AND AUXILIARY DATA TRANSMISSION OVER A SERIAL LINK	AHN, GIJUNG
<a href="#">10305254</a>	Not Issued	161	11/25/2002	0.6-2.5 GBaud CMOS tracked 3X oversampling transceiver with dead zone phase detection for robust clock/data recovery	AHN, GIJUNG
<a href="#">10356695</a>	<a href="#">6859107</a>	150	01/30/2003	FREQUENCY COMPARATOR WITH HYSTERESIS BETWEEN LOCKED AND UNLOCKED CONDITIONS	AHN, GIJUNG
<a href="#">10612840</a>	Not Issued	30	07/03/2003	Tracked 3X oversampling receiver	AHN, GIJUNG
<a href="#">10613442</a>	<a href="#">6888417</a>	150	07/03/2003	VOLTAGE CONTROLLED OSCILLATOR	AHN, GIJUNG
<a href="#">10658590</a>	Not Issued	30	09/08/2003	Method and apparatus for double data rate serial ATA phy interface	AHN, GIJUNG
<a href="#">10722842</a>	<a href="#">6876240</a>	150	11/25/2003	WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP	AHN, GIJUNG
<a href="#">10781405</a>	Not Issued	71	02/18/2004	Cable with circuitry for asserting stored cable data or other information to an external device or user	AHN, GIJUNG
<a href="#">60058040</a>	Not Issued	159	09/04/1997	DATA RECOVERY SCHEME FOR OVERSAMPLED SYSTEMS	AHN, GIJUNG
<a href="#">60071879</a>	Not Issued	159	01/20/1998	1.25GBAUD CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABIT ETHERNET PHY CHIP	AHN, GIJUNG
<a href="#">60230589</a>	Not Issued	159	09/05/2000	Oversampling transceiver with dead-zone phase detection	AHN, GIJUNG
<a href="#">60333439</a>	Not Issued	159	11/26/2001	0.6-2.5GBaud CMOS tracked 3x oversampling transceiver with dead-zone phase detection for robust clock/data recovery	AHN, GIJUNG
<a href="#">60406858</a>	Not Issued	159	08/29/2002	CMOS transceiver with dual current path VCO	AHN, GIJUNG
<a href="#">60760601</a>	Not Issued	20	01/20/2006	Concurrent code checker: hardware efficient HSIO built-in self-test & debug structure	AHN, GIJUNG

Inventor Search Completed: No Records to Display.

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## Inventor Name Search Result

Your Search was:

Last Name = JEONG

First Name = DEOG-KYOON

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">08000430</a>	<a href="#">5332934</a>	150	01/04/1993	SMALL TO FULL SWING CONVERSION CIRCUIT	JEONG, DEOG-KYOON
<a href="#">08254326</a>	<a href="#">5714904</a>	150	06/06/1994	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
<a href="#">08332561</a>	<a href="#">5574756</a>	150	10/31/1994	METHOD FOR GENERATING DIGITAL COMMUNICATION SYSTEM CLOCK SIGNALS & CIRCUITRY FOR PERFORMING THAT METHOD	JEONG, DEOG-KYOON
<a href="#">08370904</a>	<a href="#">5621407</a>	150	01/10/1995	DIGITAL/ANALOG CONVERTER	JEONG, DEOG-KYOON
<a href="#">08415056</a>	<a href="#">5712884</a>	150	03/31/1995	DATA RECEIVING METHOD AND CIRCUIT OF DIGITAL COMMUNICATION SYSTEM	JEONG, DEOG-KYOON
<a href="#">08580569</a>	<a href="#">5705947</a>	150	12/29/1995	CLOCK GENERATOR	JEONG, DEOG-KYOON
<a href="#">08580571</a>	<a href="#">5587709</a>	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
<a href="#">08580700</a>	<a href="#">5675584</a>	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
<a href="#">08580914</a>	<a href="#">5712585</a>	150	12/29/1995	A SYSTEM FOR DISTRIBRITING CLOCK SIGNALS	JEONG, DEOG-KYOON
<a href="#">08581135</a>	<a href="#">5802103</a>	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
<a href="#">08631420</a>	<a href="#">5815041</a>	150	04/12/1996	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	JEONG, DEOG-KYOON
<a href="#">08664136</a>	<a href="#">5835498</a>	150	06/14/1996	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK	JEONG, DEOG-KYOON
<a href="#">08815486</a>	<a href="#">6157360</a>	150	03/11/1997	SYSTEM AND METHOD FOR DRIVING COLUMNS OF AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
<a href="#">08920336</a>	<a href="#">5955929</a>	150	08/27/1997	VOLTAGE-CONTROLLED OSCILLATOR RESISTANT TO SUPPLY VOLTAGE NOISE	JEONG, DEOG-KYOON
<a href="#">08937262</a>	<a href="#">6100868</a>	150	09/15/1997	HIGH DENSITY COLUMN DRIVERS FOR AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
<a href="#">09007707</a>	<a href="#">5969552</a>	150	01/15/1998	DUAL LOOP DELAY-LOCKED LOOP	JEONG, DEOG-KYOON
<a href="#">09013679</a>	<a href="#">6211714</a>	150	01/26/1998	PARALLEL CONDUCTOR SYSTEM FOR REDUCING NOISE IN TRANSMITTING CLOCK SIGNALS	JEONG, DEOG-KYOON
<a href="#">09017758</a>	<a href="#">6107946</a>	150	02/03/1998	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
<a href="#">09098266</a>	<a href="#">6157263</a>	150	06/16/1998	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	JEONG, DEOG-KYOON
<a href="#">09146818</a>	<a href="#">6229859</a>	150	09/04/1998	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	JEONG, DEOG-KYOON
<a href="#">09148583</a>	<a href="#">6271816</a>	150	09/04/1998	POWER SAVING CIRCUIT AND METHOD FOR DRIVING AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
<a href="#">09148815</a>	<a href="#">6144242</a>	150	09/04/1998	CONTROLLABLE DELAYS IN MULTIPLE SYNCHRONIZED SIGNALS FOR REDUCED ELECTROMAGNETIC INTERFERENCE AT PEAK FREQUENCIES	JEONG, DEOG-KYOON
<a href="#">09187559</a>	<a href="#">6151334</a>	150	11/04/1998	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK	JEONG, DEOG-KYOON
<a href="#">09234619</a>	<a href="#">6560290</a>	150	01/20/1999	CMOS DRIVER AND ON-CHIP TERMINATION FOR	JEONG, DEOG-KYOON



				GIGABAUD SPEED DATA COMMUNICATION	
<a href="#">09234777</a>	<a href="#">6600771</a>	150	01/20/1999	SPREAD SPECTRUM PHASE MODULATION FOR SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS	JEONG, DEOG-KYOON
<a href="#">09298369</a>	<a href="#">6374361</a>	150	04/22/1999	SKEW-INSENSITIVE LOW VOLTAGE DIFFERENTIAL RECEIVER	JEONG, DEOG-KYOON
<a href="#">09393849</a>	<a href="#">6738417</a>	150	09/09/1999	METHOD AND APPARATUS FOR BIDIRECTIONAL DATA TRANSFER BETWEEN A DIGITAL DISPLAY AND A COMPUTER	JEONG, DEOG-KYOON
<a href="#">09574571</a>	<a href="#">6326826</a>	150	05/17/2000	Wide frequency-range delay-locked loop circuit	JEONG, DEOG-KYOON
<a href="#">09693516</a>	<a href="#">6462624</a>	150	10/20/2000	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP	JEONG, DEOG-KYOON
<a href="#">09709637</a>	<a href="#">6483355</a>	150	11/13/2000	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	JEONG, DEOG-KYOON
<a href="#">09759624</a>	<a href="#">6891910</a>	150	01/12/2001	BAUD-RATE TIMING RECOVERY	JEONG, DEOG-KYOON
<a href="#">09766503</a>	Not Issued	160	01/18/2001	High speed serial link for fully duplexed data communication	JEONG, DEOG-KYOON
<a href="#">09814256</a>	<a href="#">6587525</a>	150	03/21/2001	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	JEONG, DEOG-KYOON
<a href="#">09897975</a>	<a href="#">6510185</a>	150	07/05/2001	SINGLE CHIP CMOS TRANSMITTER/RECEIVER	JEONG, DEOG-KYOON
<a href="#">09943029</a>	Not Issued	161	08/29/2001	Data recovery using data eye tracking	JEONG, DEOG-KYOON
<a href="#">09948123</a>	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	JEONG, DEOG-KYOON
<a href="#">09985897</a>	<a href="#">6512408</a>	150	11/06/2001	MIXER STRUCTURE AND METHOD FOR USING SAME	JEONG, DEOG-KYOON
<a href="#">10035591</a>	Not Issued	41	11/07/2001	Communications architecture for storage-based devices	JEONG, DEOG-KYOON
<a href="#">10035911</a>	Not Issued	95	11/07/2001	METHOD AND SYSTEM FOR NESTING OF COMMUNICATIONS PACKETS	JEONG, DEOG-KYOON
<a href="#">10036135</a>	Not Issued	61	11/07/2001	Method and system for packet ordering based on packet type	JEONG, DEOG-KYOON
<a href="#">10036794</a>	<a href="#">6976201</a>	150	11/07/2001	METHOD AND SYSTEM FOR HOST HANDLING OF COMMUNICATIONS ERRORS	JEONG, DEOG-KYOON
<a href="#">10037168</a>	Not Issued	61	11/07/2001	Method and system for plesiosynchronous communications with null insertion and removal	JEONG, DEOG-KYOON
<a href="#">10045297</a>	Not Issued	71	11/07/2001	Communications architecture for memory-based devices	JEONG, DEOG-KYOON
<a href="#">10045348</a>	Not Issued	41	11/07/2001	Method and system for asymmetric packet ordering between communications devices	JEONG, DEOG-KYOON
<a href="#">10045393</a>	<a href="#">7039121</a>	150	11/07/2001	METHOD AND SYSTEM FOR TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION COMMUNICATIONS	JEONG, DEOG-KYOON
<a href="#">10045600</a>	<a href="#">6771192</a>	150	11/07/2001	METHOD AND SYSTEM FOR DC-BALANCING AT THE PHYSICAL LAYER	JEONG, DEOG-KYOON
<a href="#">10045601</a>	Not Issued	121	11/07/2001	Multisection memory bank system	JEONG, DEOG-KYOON
<a href="#">10045606</a>	Not Issued	161	11/07/2001	Method and system for dynamic segmentation of communications packets	JEONG, DEOG-KYOON
<a href="#">10045625</a>	Not Issued	41	11/07/2001	Method and system for integrating packet type information with synchronization symbols	JEONG, DEOG-KYOON
<a href="#">10053461</a>	<a href="#">7113507</a>	150	11/07/2001	METHOD AND SYSTEM FOR COMMUNICATING CONTROL INFORMATION VIA OUT-OF-BAND SYMBOLS	JEONG, DEOG-KYOON

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